IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. . . . . Filed herewith
Filing Date . . . . . Filed herewith
Inventor . . . . . Ji Ung Lee et al.
Assignee . . . . . Micron Technology, Inc.
Group Art Unit . . . . . Unknown
Examiner . . . . . Unknown
Attorney's Docket No. MI30-068
Title: "Field Effect Transistor Fabrication Methods, Field Emission Device Fabrication Methods, and Field Emission Device Operational Methods"

PRELIMINARY AMENDMENT

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

EL 844504097

From: James D. Shaurette (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

Please enter the following amendments prior to examining the above-identified application:

AMENDMENTS

In the Title:

Please replace the title with the following: –FIELD EFFECT TRANSISTOR FABRICATION METHODS, FIELD EMISSION DEVICE FABRICATION METHODS, AND FIELD EMISSION DEVICE OPERATIONAL METHODS–.

In the Specification

At page 1 before the "Technical Field" section please insert:

--RELATED PATENT DATA

This patent resulted from a continuation of and claims priority to U.S. Patent Application Serial No. 09/260,231, filed on March 1, 1999, entitled "Field Effect Transistors, Field Emission Apparatuses, Thin Film Transistors, and Methods of Forming Field Effect Transistors", now U.S. Patent No. 6,344,378, naming Ji Ung Lee and John Kichul Lee as inventors, the disclosure of which is incorporated herein by reference.--.

In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. § 1.121(c)(1)(i).

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. § 1.121(c)(1)(ii).

74. (New) A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a source semiconductive region and a drain semiconductive region adjacent to the channel region of the semiconductive material, and wherein the providing the drain semiconductive region comprises providing at least one emitter;

providing gate dielectric material over the channel region; and

providing a gate over the gate dielectric material and the channel region.

75. (New) The method of claim 74 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

76. (New) The method of claim 74 wherein the providing the gate comprises polishing the gate dielectric material and gate material to form the gate aligned with the channel region of the semiconductive material.

77. (New) The method of claim 74 wherein the providing the at least one emitter comprises providing a plurality of emitters.

78. (New) The method of claim 74 wherein the providing the gate comprises providing the gate about the emitter.

79. (New) A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a plurality of semiconductive regions adjacent to the channel region of the semiconductive material; and

self-aligning a gate with the semiconductive regions after the providing the semiconductive regions.

80. (New) The method of claim 79 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

81. (New) The method of claim 79 further comprising:

providing gate dielectric material over the channel region; and

providing gate material over the gate dielectric material;

wherein the self-aligning comprises polishing the gate dielectric material and the gate material.

82. (New) The method of claim 79 further comprising providing gate dielectric material over the channel region and the gate dielectric material including an upper surface substantially elevationally coincident with an upper surface of the gate.

83. (New) A field emission device fabrication method comprising:

providing semiconductive material;

providing a plurality of semiconductive regions adjacent to the semiconductive material, and wherein the providing the semiconductive regions comprises providing one of the semiconductive regions comprising an emitter; and

providing a gate intermediate the semiconductive regions.

84. (New) The method of claim 83 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

85. (New) The method of claim 83 wherein the providing the semiconductive regions and the providing the gate comprise forming a field effect transistor.

86. (New) The method of claim 83 wherein the providing one of the semiconductive regions comprising an emitter comprises forming a tip of the emitter elevationally below an upper surface of the gate and an upper surface of another one of the semiconductive regions.

87. (New) The method of claim 83 wherein the providing one of the semiconductive regions comprising an emitter comprises providing a plurality of emitters.

88. (New) The method of claim 83 wherein the providing the gate comprises providing the gate about the emitter.

89. (New) A field emission device operational method comprising:

providing a plurality of semiconductive regions adjacent to a channel region, and wherein at least one of the semiconductive regions comprises an emitter; and

controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive regions.

90. (New) The method of claim 89 wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to semiconductive material comprising a semiconductive layer.

91. (New) The method of claim 89 wherein the providing the semiconductive regions comprises providing the semiconductive regions adjacent to semiconductive material comprising a thin film semiconductive layer.

92. (New) The method of claim 89 further comprising configuring the gate and the semiconductive regions to form a field effect transistor.

93. (New) A field effect transistor fabrication method comprising:

providing spaced semiconductive regions;

providing a channel region within semiconductive material between the spaced semiconductive regions;

providing gate dielectric material over the channel region; and

providing a gate intermediate the semiconductive regions and over the channel region;

wherein the gate dielectric layer has an upper surface elevationally coincident with an upper surface of the gate.

94. (New) The method of claim 93 further comprising providing the semiconductive material comprising a thin film conductive layer.

95. (New) The method of claim 93 wherein the semiconductive regions comprise an upper surface substantially elevationally coincident with an upper surface of the gate.

96. (New) The method of claim 93 wherein the providing the gate comprises polishing gate material and the gate dielectric material.

97. (New) A field effect transistor fabrication method comprising:

providing a plurality of semiconductive regions with a channel region therebetween;

providing a gate dielectric layer over the channel region; and

providing a gate over the gate dielectric layer;

wherein the providing the gate comprises aligning the gate with the channel region using the gate dielectric layer.

98. (New) The method of claim 97 further comprising providing semiconductive material comprising the channel region.

99. (New) The method of claim 98 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

100. (New) The method of claim 97 wherein the providing the gate comprises forming a gate layer over the gate dielectric layer, and the aligning comprises removing portions of the gate dielectric layer and the gate layer.

101. (New) The method of claim 97 wherein the providing the semiconductive regions comprises providing at least one of the semiconductive regions comprising a field emitter.

102. (New) A field effect transistor fabrication method comprising:

providing semiconductive material including a channel region;

providing a plurality of semiconductive regions adjacent to the channel region of the semiconductive material; and

providing a gate comprising gate material over the channel region of the semiconductive material without the use of a mask over the gate material.

103. (New) The method of claim 102 wherein the providing the semiconductive material comprises providing a thin film semiconductive layer.

104. (New) The method of claim 102 further comprising providing gate dielectric material over the semiconductive material, and wherein the providing the gate comprises aligning the gate with the channel region of the semiconductive material using gate dielectric material.

105. (New) The method of claim 102 wherein the providing the gate comprises removing portions of the gate material to self-align the gate with the channel region of the semiconductive material.

106. (New) The method of claim 102 further comprising providing gate dielectric material over the semiconductive material, and wherein an upper surface of the gate dielectric material is substantially elevationally coincident with an upper surface of the gate.

107. (New) The method of claim 102 wherein the providing the semiconductive regions comprises providing a drain region comprising a field emitter.

108. (New) A field effect transistor fabrication method comprising:

providing spaced semiconductive regions including a channel region positioned therebetween;

providing gate material and gate dielectric material over the channel region; and

polishing the gate dielectric material and the gate material to form a gate intermediate the spaced semiconductive regions over the channel region.

109. (New) The method of claim 108 wherein the polishing aligns the gate with the channel region.

110. (New) The method of claim 108 wherein the providing the semiconductive regions comprises providing a drain comprising a field emitter.

111. (New) The method of claim 108 wherein the polishing comprises chemical-mechanical polishing.

REMARKS

This application is a continuation application of U.S. Patent Application Serial No. 09/260,231, filed on March 1, 1999. Claims 1-73 have been canceled without prejudice. Claims 74-111 are pending in the application, and Applicants request examination of such pending claims.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: 2/5/02

By: _____

James D. Shaurette
Reg. No. 39,833

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. . . . . Filed Herewith
Filing Date . . . . . Filed Herewith
Inventor . . . . . Rickie C. Lake
Assignee . . . . . Micron Technology, Inc.
Group Art Unit . . . . . Unknown
Examiner . . . . . Unknown
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Attention: Official Draftsman

EL 844504097

SUBSTITUTE DRAWING REQUEST

Please enter the enclosed substitute drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: 2/5/02

By: _____

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Enclosures: 8 Sheets of Formal Drawings, Figs. 1-17.